UNIT II

Bipolar Junction Transistors (BJT) & Junction Field Effect Transistors (JFET)

Introduction to Electronics Engineering (IEE)

Topic 1: Introduction to the Bipolar Junction Transistor (BJT)

1.1 What is a Transistor?

- Besides diodes, the transistor is the most popular semiconductor device. The most common type is the Bipolar Junction Transistor (BJT).
- Key applications of transistors: as an amplifier and as a switch.
- A transistor is a three-terminal device: Base (B), Emitter (E), and Collector (C).
- In a bipolar transistor, current conduction occurs due to both types of charge carriers — electrons and holes. Hence the name Bipolar Junction Transistor.
- In a BJT, the output current is controlled by the input current, making it a current-controlled device.

1.2 Types of BJT

- NPN Transistor — Emitter and Collector are n-doped; Base is p-doped.
- PNP Transistor — Emitter and Collector are p-doped; Base is n-doped.

Doping Levels in BJT

Emitter: Heavily doped — supplies majority carriers.

Base: Lightly doped and very thin — enables carrier transit.

Collector: Moderately doped — collects majority carriers from emitter.

1.3 Modes of Operation for BJT

Depending on the external bias voltage polarities applied to the two junctions, the transistor operates in one of three regions:

Region	Emitter-Base Junction (J_e)	Collector-Base Junction (Jc)	Application / Behaviour
Cut-off	Reverse Biased	Reverse Biased	Transistor is OFF — acts as open switch
Active	Forward Biased	Reverse Biased	Amplification region — linear operation
Saturation	Forward Biased	Forward Biased	Transistor is ON — acts as closed switch

Topic 2: Working Principles of BJT

2.1 NPN Transistor Operation

For proper amplifier operation, the Emitter-Base (EB) junction is forward biased and the Collector-Base (CB) junction is reverse biased (Active Region).

- The forward-biased EB junction causes electrons in the n-type emitter to flow toward the base, constituting Emitter Current (I_E).
- As electrons flow through the thin, lightly doped p-type base, very few recombine with holes. This small recombination constitutes Base Current (I_D).
- The remaining large number of electrons cross into the collector region and flow to the positive terminal, constituting Collector Current (Ic).
- Since most emitter electrons reach the collector, the collector current is much larger than the base current.

$$I_E = I_D + I_C$$

2.2 PNP Transistor Operation

- The forward-biased EB junction causes holes in the p-type emitter to flow toward the base, constituting Emitter Current (I_E).
- As holes flow through the thin n-type base, very few recombine with electrons, constituting Base Current (I_D).
- The remaining large number of holes cross the depletion region into the collector, constituting Collector Current (Ic).
- Hole flow is the dominant conduction mechanism in a PNP transistor.

$$I_E = I_D + I_C$$

Topic 3: BJT Configurations

3.1 Overview of Three Configurations

A BJT can be connected in three different configurations, each with unique characteristics:

Common Base (CB) Configuration

- Base terminal is common to both input and output circuits.
- Input: Emitter | Output: Collector
- High voltage gain, low input impedance, current gain < 1 (α).
- Used in high-frequency applications.

Common Emitter (CE) Configuration

- Emitter terminal is common to both input and output circuits.
- Input: Base | Output: Collector
- High voltage gain and high current gain (β).
- Output is 180° phase inverted relative to input.
- Most widely used configuration for amplification.

Common Collector (CC) Configuration — Emitter Follower

- Collector terminal is common to both input and output circuits.
- Input: Base | Output: Emitter
- High input impedance, low output impedance, approximately unity voltage gain.
- Used primarily for impedance matching and as a buffer stage.

3.2 Configuration Comparison Table

Parameter	Common Base (CB)	Common Emitter (CE)	Common Collector (CC)
Common Terminal	Base	Emitter	Collector
Input Terminal	Emitter	Base	Base
Output Terminal	Collector	Collector	Emitter
Current Gain	< 1 (α, ~0.95–0.99)	High (β, typically 20–500)	High (β + 1)
Voltage Gain	High	High	≈1 (Unity)
Input Impedance	Low (~50–0.5 kΩ)	Medium (~1 kΩ)	High (~100 kΩ)
Output Impedance	High	Medium	Low
Phase Shift (V)	0° (No inversion)	180° (Inverted)	0° (No inversion)
Primary Application	High-frequency circuits	General amplification	Impedance matching / buffer

Topic 4: Input and Output Characteristics

4.1 Common Base (CB) Configuration Characteristics

Input Characteristics of CB Configuration

The input characteristics represent I_E (emitter current) versus V_{DE} (base-emitter voltage) at constant V_{CD} (collector-base voltage).

- Since the emitter-base junction is forward biased, the characteristic curve resembles the forward bias I-V curve of a PN junction diode.
- An increase in V_{DE} reduces the barrier potential, allowing more charge carriers from the emitter into the base, rapidly increasing I_E.
- As V_{CD} increases, the depletion region widens (Early Effect), slightly reducing the effective base width. This causes a slight shift in the input characteristics.

Early Effect (Base Width Modulation)

- When reverse bias voltage V_{CD} increases, the depletion region widens, reducing the electrical base width.
- This reduces recombination in the base, so a slightly smaller V_{DE} is required to produce the same emitter current.
- Result: Input characteristic curves shift slightly with changes in V_{CD}.

Output Characteristics of CB Configuration

The output characteristics represent Ic (collector current) versus V_{CD} (collector-base voltage) at constant I_E (emitter current). Three regions exist:

Region	Description
Active Region	Collector current is approximately constant and nearly equal to emitter current. Transistor works as an amplifier here.
Saturation Region	V_{CD} is negative for NPN; a small change in V_{CD} produces a large collector current change. Both junctions are forward biased.
Cut-off Region	Corresponds to $I_E = 0$. A small leakage current (I_{CD_o}) still flows due to minority carriers even when $I_E = 0$.

4.2 Common Emitter (CE) Configuration Characteristics

Input Characteristics of CE Configuration

Represents I_D (base current) versus V_{DE} (base-emitter voltage) at constant V_{CE} (collector-emitter voltage).

- Since the BE junction is forward biased, a small increase in V_{DE} causes a significant increase in I_D.
- The curve resembles the forward-bias characteristic of a PN junction diode.
- When V_{CE} increases, the reverse bias on the CB junction increases, reducing the effective base width (Early Effect) and causing a slight shift in the curves.

Output Characteristics of CE Configuration

Represents Ic (collector current) versus V_{CE} (collector-emitter voltage) at constant I_D (base current).

- Active Region: BE junction is forward biased; CB junction is reverse biased. Ic remains nearly constant for a wide range of V_{CE} and depends mainly on I_D and β.
- Saturation Region: At very low V_{CE}, both junctions become forward biased. Ic increases rapidly with voltage.
- Cut-off Region: When $I_D = 0$, only a small leakage current I_{CE_o} flows through the collector.

$$I_C = \beta \times I_D + I_{CE_o}$$

4.3 Common Collector (CC) Configuration Characteristics

- In CC Configuration, the Collector terminal is common to both input and output.
- Input Characteristics: Variation of I_D with V_{CD} keeping V_{CE} constant.
- Output Characteristics: Variation of I_E with V_{CE} keeping I_D constant.
- The output characteristics are similar in shape to CE configuration but I_E is the output current instead of Ic.

Topic 5: Current Gains and Leakage Currents

5.1 Current Gain in Common Base Configuration (α)

The current transfer ratio α (alpha) in CB configuration is the ratio of collector current to emitter current:

$$\alpha = I_C / I_E \qquad (\alpha < 1, \text{ typically } 0.95 - 0.99)$$

CB Leakage Current (I_{CD_o})

I_{CD_o}: Collector-Base leakage current. Flows when the emitter is open-circuited and the CB junction is reverse biased.

- When $I_E = 0$, $I_C = I_{CD_o}$ (caused by thermally generated minority carriers crossing the junction).
- I_{CD_o} increases with temperature.

$$I_C = \alpha \times I_E + I_{CD_o}$$

5.2 Current Gain in Common Emitter Configuration (β)

Current gain β (beta) is the ratio of collector current to base current in CE configuration:

$$\beta = I_C / I_D \qquad (\text{typically } 20 - 500)$$

CE Leakage Current (I_{CE_o})

I_{CE_o}: Collector-Emitter leakage current. Flows when the base is open-circuited and the CB junction is reverse biased.

Derivation: Relation Between I_{CD_o} and I_{CE_o}

Starting from $I_C = \alpha I_E + I_{CD_o}$ and substituting $I_E = I_D + I_C$:

$$I_C(1 - \alpha) = \alpha I_D + I_{CD_o}$$

$$I_C = [\alpha / (1 - \alpha)] \times I_D + [1 / (1 - \alpha)] \times I_{CD_o}$$

$$I_C = \beta I_D + I_{CE_o}$$

$$I_{CE_o} = [1 / (1 - \alpha)] \times I_{CD_o} = (\beta + 1) \times I_{CD_o}$$

5.3 Relation Between α and β

$$\beta = \alpha / (1 - \alpha)$$

$$\alpha = \beta / (1 + \beta)$$

$$\text{Note: } 1 / (1 - \alpha) = \beta + 1$$

5.4 Current Gains Summary Table

Parameter	Symbol	Formula	Typical Value
CB Current Gain	α (alpha)	$\alpha = I_C / I_E$	0.95 – 0.99 (< 1)
CE Current Gain	β (beta)	$\beta = I_C / I_D$	20 – 500
Relation: β from α	β	$\beta = \alpha / (1 - \alpha)$	—
Relation: α from β	α	$\alpha = \beta / (1 + \beta)$	—
CE Leakage Current	I_{CE_o}	$I_{CE_o} = (1/(1-\alpha)) \times I_{CD_o} = (\beta+1) \times I_{CD_o}$	Much larger than I_{CD_o}
KCL at Transistor	—	$I_E = I_D + I_C$	—

Topic 6: BJT Biasing

6.1 Introduction to Biasing

- Transistor biasing is the process of setting the transistor's DC operating voltage and current conditions (Q-point) to the correct level so that any AC input signal can be amplified correctly.
- For the BJT to operate in its linear (active) region: the Base-Emitter junction must be forward-biased AND the Base-Collector junction must be reverse-biased.
- The analysis of any amplifier has two components: a DC analysis and an AC analysis.

Types of Transistor Biasing

1. Fixed Bias
2. Emitter Bias
3. Voltage Divider Bias
4. Collector Feedback Bias

6.2 Fixed Bias Method

- A single resistor R_D is connected between the base and the DC supply Vcc to provide the required base current.
- The BE junction is forward biased by the base supply; the CE circuit is powered separately.

DC Analysis — Fixed Bias

Applying Kirchhoff's Voltage Law (KVL) to the base-emitter loop:

$$+V_{CC} - I_D \times R_D - V_{DE} = 0$$

Solving for base current:

$$I_D = (V_{CC} - V_{DE}) / R_D$$

Collector current from base current:

$$I_C = \beta \times I_D$$

Applying KVL to the collector-emitter loop:

$$V_{CE} + I_C \times R_C - V_{CC} = 0$$

$$V_{CE} = V_{CC} - I_C \times R_C$$

Since $V_E = 0$ V (emitter grounded):

$V_{CE} = V_C$ and $V_{DE} = V_D$

6.3 Load-Line Analysis and the Q-Point

- Load line analysis is a graphical method used to determine the operating point (Q-point) of a transistor on its output characteristics.
- The DC load line shows all possible combinations of I_C and V_{CE} for a given V_{CC} and R_C.
- The load line equation is derived from: $V_{CE} = V_{CC} - I_C \times R_C$

Finding the Two End-Points of the Load Line

When $I_C = 0$ mA: $V_{CE} = V_{CC}$ → This gives the voltage intercept on the x-axis.

When $V_{CE} = 0$ V: $I_C = V_{CC} / R_C$ → This gives the current intercept on the y-axis.

Q-Point (Quiescent Point): The point where the DC load line intersects the transistor output characteristic for a specific base current I_D. This is the DC operating point.

An ideal Q-point is located at the midpoint of the load line to allow maximum symmetrical signal swing without distortion or clipping.

6.4 Biasing Methods Comparison

Bias Method	Key Feature	Stability	Use Case
Fixed Bias	Single resistor R_D from Vcc to base	Poor (Q-point shifts with β)	Simple circuits, lab demos
Emitter Bias	Emitter resistor R_E added for stability	Moderate	Better stability than fixed
Voltage Divider Bias	Two resistors (R_1 , R_2) form a voltage divider	Excellent (most stable)	Most widely used in practice
Collector Feedback Bias	Feedback resistor from collector to base	Good (self-stabilizing)	Single-supply circuits

Topic 7: Junction Field Effect Transistor (JFET)

7.1 Introduction to Field Effect Transistors

- A Field Effect Transistor (FET) is a voltage-controlled device — the output characteristics are controlled by the input voltage (not current).
- There are two basic types of FETs:
  - Junction Field Effect Transistor (JFET)
  - Metal Oxide Semiconductor Field Effect Transistor (MOSFET)

7.2 JFET — Definition and Structure

- A JFET is a three-terminal semiconductor device in which current conduction is by one type of carrier only (electrons OR holes) — hence it is a unipolar device.
- Terminals: Source (S), Drain (D), and Gate (G).
- Current conduction is controlled by an electric field between the gate and the conducting channel.
- Two types: N-channel JFET (more common) and P-channel JFET.

7.3 Construction of JFET (N-Channel)

- An N-type silicon bar (the channel) has two smaller pieces of P-type silicon diffused on opposite sides of its middle section, forming two P-N junctions.
- The two P-N junctions are connected internally and a common gate terminal (G) is brought out.
- Ohmic contacts are made at the two ends of the N-channel:

Source (S): Terminal through which majority carriers (electrons for N-channel) enter the channel.

Drain (D): Terminal through which majority carriers leave the channel.

Channel: The region between Source and Drain, sandwiched between the two gate regions, through which majority carriers flow.

Gate (G): Controls the width of the channel using a reverse-biased PN junction and hence controls the drain current.

7.4 Working Principle of JFET

- The gate is always reverse biased relative to the source, creating depletion layers on both sides of the channel.
- When V_{DD} is applied between drain and source (with V_{G} = 0), two P-N junctions establish depletion layers. Electrons flow from source to drain through the channel between the depletion layers.
- The size of the depletion layers determines the channel width and hence the drain current.
- For small V_{DD}, the N-type bar acts as a simple resistor; drain current increases linearly with V_{DD} up to the knee point.
- As V_{DD} increases further, the channel constricts more at the drain end until it is pinched off.
- Beyond pinch-off, drain current I_D no longer increases with V_D — it saturates at a constant value (I_{D} when V_{G} = 0 V).

Effect of Gate-Source Voltage (V_{G})

- Applying a more negative V_{G} (reverse bias on gate) widens the depletion layers, reducing channel width and decreasing drain current.
- Reducing the reverse bias on the gate narrows the depletion layers, widening the channel and increasing drain current.

7.5 Pinch-Off Voltage ($V_{}$)

Pinch-Off Voltage ($V_{}$): The value of V_D at which the channel is completely pinched off (all free charges removed from channel) and drain current I_D reaches a constant saturation value.

Beyond pinch-off, I_D saturates. The drain current in the pinch-off (saturation) region is given by Shockley's equation for JFET:

$$I_D = I_{D} \times (1 - V_{G} / V_{})^2$$

Symbol	Meaning
I_D	Drain current at operating point
I_{DSS}	Drain-to-Source Saturation current (maximum I_D when V_{GS} = 0 V)
V_{GS}	Gate-to-Source voltage (control input)
V_P	Pinch-off voltage (at which I_D = 0 mA)

7.6 Transfer Characteristics of JFET

The transfer characteristics show the relationship between drain current I_D and gate-source voltage V_{GS} (the control variable), derived from Shockley's equation:

$$I_D = I_{DSS} \times (1 - V_{GS} / V_P)^2$$

Key Points from Shockley's JFET Equation

When V_{GS} = 0 V:

$$I_D = I_{DSS} (1 - 0)^2 = I_{DSS} \quad \rightarrow \textbf{Maximum drain current}$$

When $V_{GS} = V_P$:

$$I_D = I_{DSS} (1 - 1)^2 = 0 \text{ mA} \quad \rightarrow \textbf{Channel fully pinched off}$$

Transfer Characteristic Reference Table

V_{GS}	I_D (Drain Current)	Notes
0 V	I_{DSS}	Maximum drain current; channel fully open
0.3 V_P	I_{DSS} / 2	Half of maximum current
0.5 V_P	I_{DSS} / 4	Quarter of maximum current
V_P (Pinch-off voltage)	0 mA	Channel fully pinched off; no drain current

7.7 Comparison: BJT vs. JFET

Parameter	BJT	JFET
Control Type	Current Controlled (I_B controls I_C)	Voltage Controlled (V_{GS} controls I_D)
Terminals	Base, Emitter, Collector	Gate, Source, Drain
Input Impedance	Low to Medium (~kΩ)	Very High (~MΩ)
Carriers	Both (electrons & holes) — Bipolar	One type only (unipolar)
Noise	Higher noise	Lower noise
Gain	High current & voltage gain	Moderate voltage gain
Control Mechanism	Base current	Gate voltage (reverse biased)
Key Equation	$I_C = \beta I_B + I_{CEO}$	$I_D = I_{DSS} (1 - V_{GS}/V_P)^2$
Applications	Amplifiers, switching, logic	Amplifiers, switches, analog circuits

Topic 8: Quick Reference — Key Formulae and Definitions

8.1 BJT Key Formulae

Quantity	Formula	Notes
KCL at Transistor	$I_E = I_D + I_C$	Valid for both NPN and PNP
CB Current Gain	$\alpha = I_C / I_E$	0.95 – 0.99 (< 1)
CE Current Gain	$\beta = I_C / I_D$	20 – 500
β from α	$\beta = \alpha / (1 - \alpha)$	—
α from β	$\alpha = \beta / (1 + \beta)$	—
Collector Current (CE)	$I_C = \beta I_D + I_{CEo}$	Includes leakage
CE Leakage	$I_{CEo} = (\beta + 1) \times I_{CDo}$	Much larger than I_{CDo}
Fixed Bias: I_D	$I_D = (V_{CC} - V_{DE}) / R_D$	$V_{DE} \approx 0.7$ V for Si
Fixed Bias: V_{CE}	$V_{CE} = V_{CC} - I_C R_C$	Active region: $V_{CE} > V_{CE(sat)}$
Load Line Intercepts	$I_{C(max)} = V_{CC}/R_C$; $V_{CE(max)} = V_{CC}$	Endpoints of DC load line

8.2 JFET Key Formulae

Quantity	Formula	Notes
JFET Drain Current (Shockley)	$I_D = I_{D□□}(1 - V_{G□}/V_{□})^2$	Saturation/pinch-off region
At $V_{G□} = 0$	$I_D = I_{D□□}$	Maximum drain current
At $V_{G□} = V_{□}$	$I_D = 0$ mA	Channel fully pinched off
At $V_{G□} = 0.3V_{□}$	$I_D = I_{D□□} / 2$	Half of max current
At $V_{G□} = 0.5V_{□}$	$I_D = I_{D□□} / 4$	Quarter of max current

8.3 Key Definitions at a Glance

BJT: Bipolar Junction Transistor — a current-controlled, three-terminal device using both electron and hole conduction.

JFET: Junction Field Effect Transistor — a voltage-controlled, three-terminal unipolar device.

α (Alpha): CB current gain = I_C / I_E; always less than 1.

β (Beta): CE current gain = I_C / I_D; typically 20–500.

Active Region: BJT operating region for linear amplification. EB forward biased; CB reverse biased.

Saturation Region: Both junctions forward biased; transistor acts as a closed switch.

Cut-off Region: Both junctions reverse biased; transistor acts as an open switch.

Q-Point: Quiescent (DC operating) point — intersection of load line and transistor characteristic for a given I_D.

Load Line: Graphical representation of all possible I_C vs V_{CE} combinations for given V_{CC} and R_C.

Pinch-Off Voltage ($V_{□}$): The gate-source voltage at which the JFET channel is completely closed and $I_D = 0$ mA.

$I_{D□□}$: Drain-Source Saturation current — maximum drain current when $V_{G□} = 0$ V.

Early Effect: Base width modulation — as V_{CD} increases, depletion region widens, reducing effective base width.

I_{CDo}: CB leakage current with emitter open. Caused by thermally generated minority carriers.

I_{CEO}: CE leakage current with base open. $I_{CEO} = (\beta + 1) \times I_{CDO}$.